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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/852,647	05/11/2001	Sahng-ik Jun	06192.0178.NPUS00	5231

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EXAMINER

DUONG, THOI V

ART UNIT	PAPER NUMBER
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2871

DATE MAILED: 07/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/852,647

Applicant(s)

JUN, SAHNG-IK

Examiner

Thoi V Duong

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 June 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-38 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 10-34 is/are allowed.
- 6) ☒ Claim(s) 1-9 and 35-38 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

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DETAILED ACTION

1. This office action is in response to the RCE, Paper No. 10, filed June 03, 2003.

Accordingly, claims 1 and 35 were amended. Currently, claims 1-38 are pending in this application.

2. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-9 and 35-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al. (USPN 6,466,289 B1).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art

under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As shown in Figs. 6 and 7, Lee et al. discloses a liquid crystal display (LCD), comprising (col. 2, lines 21-43):

a plurality of gate lines 20 formed on a substrate;

a plurality of second data lines 80 insulated from and crossing over said plurality of gate lines;

a plurality of pixel regions defined by the crossing of said plurality of gate lines and said plurality of data lines ;

a common electrode or a field-generating electrode 12 formed in each pixel region having a portion laterally spaced apart from said data line with a gap therebetween;

a pixel electrode 65 formed in each pixel region, spaced apart from said common electrode with a predetermined distance therebetween;

a thin film transistor provided to each pixel region and including a semiconductor pattern 40 (col. 3, lines 61-64); and

a light interception pattern 64 of a first data line 60 formed of the same layer as the semiconductor pattern on a gate insulating layer 30 and overlapping the gap,

wherein the light interception pattern is overlapped with the corresponding data line, and the common electrode close to the corresponding data line 60 (Fig. 7);

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wherein the light interception pattern is overlapped with the common electrode 12;

wherein the semiconductor pattern is connected to the corresponding light interception pattern via a source electrode 61 (Fig. 3);

wherein the semiconductor pattern is extended to the bottom of the corresponding data line 80 (Fig. 6)

wherein the common electrodes are formed at the same plane as the gate lines (col. 3, lines 14-29);

where the pixel electrode is formed on the same plane as the first data line 60;

wherein the pixel electrode are formed at the plane different from the second data lines 80;

wherein the light interception pattern 64 is wider than the data line 80; and

wherein the light interception pattern is extended to the periphery of the corresponding data line 80.

Allowable Subject Matter

5. Claims 10-34 are allowed.

The following is an examiner's statement of reasons for allowance:

None of the prior art of record suggests or discloses that a liquid crystal display comprises "*a light interception pattern formed of the same material as said semiconductor pattern on the gate insulating layer.*"

The most revelant reference, USPN 5,247,289 of Matsueda, fails to disclose or suggest a light interception pattern formed of the same material as the semiconductor

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pattern. The Matsueda's reference discloses a portion of an amorphous silicon layer formed on top of a common electrode; however, this portion does not function as a light intercepting pattern.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion


6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (703) 308-3171. The examiner can normally be reached on Monday-Friday from 8:00 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached at (703) 305-3492.

Thoi Duong



06/29/2003



ROBERT H. KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2000